Bundesministerium für Bildung und Forschung

Deutsche Forschungsgemeinschaft DFG

2nd German Verification Day

GVD 2006

August 31, 2006

Satellite Workshop to CONCUR 2006

Universität Bonn, Germany

http://www.avacs.org/gvd/2006

The two German top projects on verification and analysis of embedded systems, the DFG funded long-term research project AVACS, a Transregional Collaborative Research Center (SFB/TR), and the BMBF funded applied research project VERISOFT, are presenting selected results from their research, within the second German Verification Day, on August 31, 2006, in Bonn, Germany. Whereas AVACS' research challenge is of foundational nature, developing novel verification algorithms covering the design space of complex embedded systems, Verisoft´s challenge is to achieve fully verified components for industry-critical systems, employing state-of-art automatic and interactive verification tools.

The foundational project AVACS (www.avacs.org) combines the expertise in formal verification at its three sites Freiburg, Oldenburg, and Saarbrücken to address the rigorous mathematical analysis of models of complex safety critical computerized systems, such as aircrafts, trains, cars, or other artifacts, whose failure can endanger human life. AVACS aims at raising the state of the art in automatic verification and analysis techniques of such complex systems from its current level of applicability to isolated points in the design space of such systems to a level allowing a comprehensive, holistic, and ultimately automatic verification of such systems, with research activities structured into three key project areas, addressing verification of real-time systems, hybrid systems, and holistic system verification, respectively.

The VERISOFT project (www.verisoft.de) combines the expertise of key industrial (BMW, Infineon, T-Systems) and academic teams to achieve fully verified key application components, covering the full design layer from applications to hardware, strengthening the competitive positioning in the addressed industrial sectors by being able to offer fully formally verified components. To this end, formal mathematical proofs will be rigorously established using a combination of state-of-the-art interactive and automatic verification methods.

Werner Damm
Carl von Ossietzky Universität Oldenburg

Wolfgang Paul
Universität des Saarlandes

Co-Organizers

Program

Wednesday, August 30 2006

19:00 **Reception and Pre-Event Dinner**
at the *Parkrestaurant RheinAue*

Invited Dinner speech
Engineering and science, a collusion of cultures
Tony Hoare, Microsoft Research

Thursday, August 31 2006

08:30 – 09:00 **Welcome**
Werner Damm, CvO Universität Oldenburg
Wolfgang Paul, Universität des Saarlandes
Christine Petry, DFG

09:00 – 09:30 **Survey Talk**
The SFB/TR AVACS
Werner Damm, CvO Universität Oldenburg

09:30 – 10:30 **Selected Presentations from AVACS**

Verifying real-time aspects of the European Train Control System
Johannes Faber, CvO Universität Oldenburg

A tight integration of SAT and interval constraint propagation
Martin Fränzle, CvO Universität Oldenburg

10:30 – 11:00 **Coffee Break**

11:00 – 12:00 **Selected Presentations from AVACS**

Verifying Partial Designs
Sven Schewe, Universität des Saarlandes

Platoon Modelling and Verification
Jörg Bauer, Universität des Saarlandes

12:00 – 12:45 **Invited Presentation**

Recent Advances in Probabilistic Model Checking
Joost-Pieter Katoen, RWTH Aachen

12:45 – 14:00 **Lunch Break**

14:00 – 14:45 **Invited Presentation**

Industrialisation of Formal Methods in System Development
Gert Döhmen, Airbus D

14:45 – 15:30 **Invited Presentation**

Mathematics-Based IP
Warren A. Hunt, Jr., The University of Texas at Austin

15:30 – 16:00 **Survey Talk**

The BMBF Project Verisoft
Wolfgang Paul, Universität des Saarlandes

16:00 – 16:30 **Coffee Break**

16:30 – 18:30 **Selected presentations from Verisoft**

Validating C-to-Assembler Translations
Lars Kuhtz, Universität des Saarlandes

Improving ISABELLE in the Verisoft Context
Tobias Nipkow, TU München

Automation and Robustness of Correctness Proofs for Processors
Wolfgang Büttner, OneSpin Solutions

Status Report: The Formal Verification of a Distributed Realtime System
Steffen Knapp, Universität des Saarlandes

18:30 **End**